Remarks

Claims 47-66 are pending in this application. Claims 47-63 are withdrawn from consideration. Claims 64-66 stand rejected.

Claims 1-46 have been cancelled.

New claim 67 has been added.

The present invention is directed to a wafer having a two layer backside seal. The two layer backside seal is designed to prevent auto doping, haze on the front side and warping of the wafer. The design comprises a low stress LPPECVD-LTO layer adjacent to the first major side of the wafer substrate and a high stress LPPECVD-LOT layer adjacent to the second major side of the low stress LPPECVD-LTO layer. The stress of the high stress LPPECVD-LTO layer is less than 300 MPa and higher than the stress of the low stress LPPECVD-LTO layer and the stress of the low stress LPPECVD-LTO layer is less than 100 MPas.

Claim Rejections - 35 U.S.C. § 112

Claims 64-66 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Applicants respectfully traverse the present rejection for the following reasons. The Examiner has objected to the term "LTO" as being indefinite. However, this term is well known in the art of thin film coatings. For example, Korman et al. (US 5,234,851) which is cited in the Office Action, uses LTO in the same manner as the claimed invention (cf. col. 8, lines 46-48). Moreover, the terms LTO (low temperature oxide) and HTO (high temperature oxide) indicate whether a silicon dioxide layer was produced under low temperature

conditions (LTO) or under high temperature conditions (HTO). The method for producing HTO is known as thermal oxidation. The most suitable method for producing LTO is Low Pressure Plasma Enhanced CVD (LPPECVD). The article, "*Silicon Dioxide Layering Methods*" (attached as Exhibit A) provides further evidence that the term "LTO" is a term of art that is readily understood in the thin film coating industry. Claim 1 is amended to further define the nature of the LTO by replacing "LTO" with "LPPECVD-LTO". The antecedent basis for this amendment is found in the Specification at page 1, lines 3-5 of the specification.

Accordingly, claim 64 is allowable under 35 U.S.C. § 112, second paragraph.

Claims 65 and 66 are rejected for being dependent upon a base rejected claim.

For the reasons set forth above, claims 65 and 66 are also allowable under the present rejection.

Claim Rejections - 35 U.S.C. § 102

Claims 64-66 are rejected under 35 U.S.C. § 102(b) as being anticipated by Korman et al. (US 5,234,851).

Applicants respectfully traverse the present rejection for the following reasons. Korman et al. discloses the structure of a field effect transistor. The structure shown in Figure 2P includes a first LTO layer 160 grown on titanium silicide and a second LTO layer 162 on top of the first one. Both layers are deposited and densified in a similar manner. Korman et al. does not disclose a structure in which the layers differ in their stress properties as required by claim 64. In particular, Korman et al. does not disclose a structure with a first LTO layer and a second LTO layer in which the stress of the second LTO layer is higher than the stress of the first LTO layer.

Accordingly, claims 64-66 are allowable under 35 U.S.C. § 102(b) over Korman et al.

Claims 64 and 66 are rejected under 35 U.S.C. § 102(b) as being anticipated by Takimazawa et al. (US 5,998,283).

Applicants respectfully traverse the present rejection for the following reasons. Takamizawa et al. discloses a silicon wafer having a CVD film formed on one face. The film is a protective film for improving gettering and for preventing autodoping (col. 2, line 67 to col. 3, line 1). The film has the property that the components and/or the composition change in a direction along the thickness of the film (col. 3, lines 10-12). The Office Action alleges that varied concentrations of oxygen will result in a variance in stress. However, Takimazawa et al. does not provide any support for this allegation. Significantly, Takimazawa et al. is also silent about whether stress is increasing or decreasing with increasing of the oxygen concentration. In particular, claim 64 requires that "the stress in the low stress LPPECVD-LTO layer is less than 100 MPa and the stress in the high stress LPPECVD-LTO layer is less than 300 MPa and the stress in the high stress LPPECVD-LTO layer is higher than the stress in the low stress LPPECVD-LTO layer." Finally, it should be appreciated that the present invention provides a multilayer structure. In contrast, Takimazawa et al. provides a **single** film having a continuous composition change. Such a configuration only becomes a multi-layer structure if the components are changed. In this regard, the disclosure is restricted to a structure in which an amorphous silicon layer and a SiO_x layer are alternatively stacked (col. 3, lines 28-31).

Accordingly, claims 64 and 66 are allowable under 35 U.S.C. § 102(b) over Takimazawa et al.

Conclusion

Applicants have made a genuine effort to respond to each of the Examiner's objections and rejections in advancing the prosecution of this case. Applicants believe that all formal and substantive requirements for patentability have been met and that this case is in condition for allowance, which action is respectfully requested. If any additional issues need to be resolved, the Examiner is invited to contact the undersigned at his earliest convenience.

Please charge any fees or credit any overpayments as a result of the filing of this paper to our Deposit Account No. 02-3978.

Respectfully submitted,

JIN-XING LI ET AL.

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EXHIBIT A

Silicon Dioxide Layering Methods

Alwin Tareen

Paper 1 from Dr. P. C. Cheng's EE548: Microelectronic Device Fabrication
University at Buffalo, Fall 2002

Converted to LaTeX on July 10, 2006

Methods for the Generation of Thin Film Insulating Layers on Silicon Wafers

Abstract

This paper comprehensively reviews the two techniques that are generally used for depositing a layer of insulating material on a silicon wafer. These techniques, thermal oxidation and chemical vapor deposition (CVD) are two general categories that encompass many distinct methodologies. The two members of the thermal oxidation category that will be covered are dry thermal oxidation and wet thermal oxidation. In the chemical vapor deposition family, there are three members that I will focus on: low-pressure CVD, atmospheric pressure CVD and plasma-enhanced CVD. For each of these methodologies, the chemistry process technology will be discussed. Also, they will be compared with each other to determine which one is suitable for a particular fabrication scenario.

Introduction

Integrated circuit fabrication is a difficult and complicated process. The physical structures involved are so delicate that many of the processing steps have to be specifically tuned to minimize the collateral damage to the wafer, sometimes at the expense of throughput. For these processing steps, many different techniques must be researched and tested, in order to discover the most effective one. This paper focuses on the process of applying a thin film of insulation to a silicon wafer. There are several different techniques that will accomplish this task, but only certain ones are effective in the harsh fabrication environment. Also, one has to respect the fact that we are dealing with an industry, and there are economic issues to consider as well. For instance, the time to completion of a process carries considerable weight, as well as up-front investment costs in equipment and infrastructure. In selecting the best layering technique, one has to balance all of these variables and make a judgement as to which one would ultimately be the best. After all, maximizing the product yield is the main goal of the semiconductor industry.

Properties of Silicon Dioxide

One of the most popular insulators in the semiconductor industry is silicon dioxide. It has been in use from the IC pioneering years of the 1970's right up until the present. Very high quality layers of silicon dioxide can be readily grown on a pure silicon surface to form a native oxide, and this

easy layer formation helped jump-start the industry in its early, non-pristine days. Silicon dioxide is available in several forms, but the one most commonly used in semiconductor technology is amorphous silicon dioxide, and this is stable at room temperature and pressure. Its dielectric constant is measured as $k = 3.9$, and this makes silicon dioxide suitable for use as a capacitor dielectric. The insulating properties of this material are such that its breakthrough field strength is very high. Even for a thin film of silicon dioxide, this value can reach 15MV/cm. Since it is so stable and chemically inert, it can protect the entire wafer region of pure silicon from the fabrication environment. The layer growth is very consistent, and it conforms readily to whatever geometries lie beneath it. Another advantage of silicon dioxide is that it can be removed from certain regions of the wafer, and the removal process won't destroy the delicate devices beneath the oxide layer. The following table outlines the general properties of silicon dioxide.

Silicon Dioxide Properties

Energy gap E_g = 8eV
Dielectric strength = between 5 and 10^6 V/cm
Dielectric constant $k = 3.9$
Density = 2.3 g/cm^3
Refractive index $n = 1.46$
Melting point = 1700°C

Thermal Oxidation

Description

This is the process by which a layer of silicon dioxide is grown on a pure silicon wafer. Prior to the chemical reaction, the wafers must be cleaned using very pure deionized water and various low-particle chemicals, to ensure a high yield. Generally, a batch of wafers are placed in an oxidation furnace, through which pure oxygen or water vapor is introduced. Heat is used as a catalyst. Thermal oxidation can grow many different types of application-specific oxide, such as gate oxide, capacitor dielectric and field oxide.

Dry Thermal Oxidation

In this process, pure oxygen and silicon are used as the reactants. A temperature of 800 – 1100°C must be maintained, since heat is a catalyst. The reaction is defined by:

$$Si_{(s)} + O_{2(g)} \longrightarrow SiO_{2(s)} \quad (1)$$

This reaction proceeds slowly, but the silicon dioxide layer growth can be controlled very accurately. Therefore, this reaction is used mostly for growing the thin gate oxide of a transistor.

Wet Thermal Oxidation

This is similar to the dry thermal oxidation process, but instead of oxygen, pure water vapor is used. The reaction is:

$$Si_{(s)} + 2H_2O_{(g)} \longrightarrow SiO_{2(s)} + 2H_{2(g)} \quad (2)$$

In this case, the reaction proceeds about ten times faster than the dry thermal oxidation. It is used mainly for generating the thick field oxide layer, which is the lateral insulation between transistors.

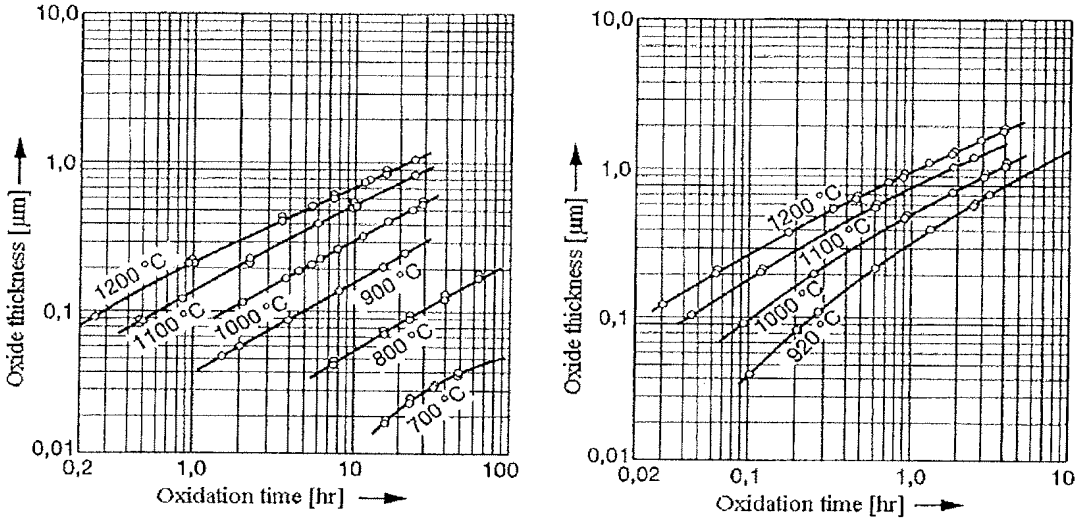

Figure 1: The Oxidation Rates of Silicon

Process Technology

In order to make it economically viable, thermal oxidation is performed on batches of wafers, typically 100 or so at a time. The oxidation furnace consists of a long quartz tube(about 2m) surrounded by heating elements, with gas inlet openings for the reactant vapors. An intricate silicon carbide rod system is used to hold the wafers, and move them in and out of the furnace. At the end of this rod is an end plate used to seal the chamber, with an outlet to let unused reactants and gaseous products escape. The entire oxidation furnace and rod system must be made of extremely pure materials, because the hot silicon wafers would react with any metal contaminants in the system. The rods have to be strong enough to support the weight of the wafers and resist any bending, even at the high temperature of 1000°C. Also, the rods must move the wafers in at a consistent velocity, and they must clear the sides of the chamber to avoid producing minute contaminant particles. When commencing the process, the oxidation furnace is heated to a temperature that is much lower than the eventual process temperature. Doing so helps reduce the thermal shock that occurs when the wafers are introduced into the system. Once loaded, the temperature is gently raised at a consistent rate to the eventual process temperature. During this

time, an inert gas such as nitrogen or argon is passed through the system. Once the process temperature is reached, the desired gaseous reactant (oxygen or water vapor) may be introduced. The wafers stay in the oxidation furnace until the desired amount of silicon dioxide has been grown on the wafers. Then, the temperature is slowly and consistently decreased, and the wafers are removed from the oxidation furnace.

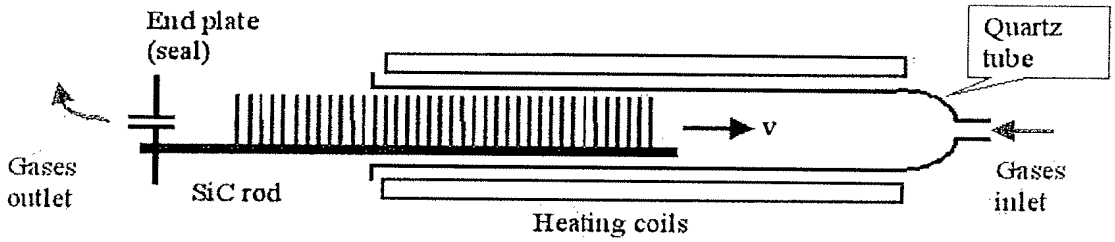

Figure 2: The Oxidation Furnace

Chemical Vapor Deposition (CVD)

Description

Deposition is defined as the change of a material from a gaseous state directly to a solid state. Here, gaseous reactant chemicals known as "precursors" are broken down at high temperatures and deposited as a thin film on the surface of a substrate. CVD is used when one needs to create a thin layer of a particular material on a substrate, but for mitigating reasons can't use thermal oxidation. One of the biggest advantages of this process is that the layers produced by CVD conform to the shape of the substrate. That is, if there were any "valleys" or "wells" etched in, the deposited layer would follow the contours of those landscapes exactly. CVD is composed of a series of general reaction steps. When the precursor vapor is introduced to the reaction vessel, it is diffused and adsorbed onto the substrate surface. Then, the precursor molecules decompose and are incorporated into a solid film. From here, the reactant byproducts are recombined and desorbed into the gaseous phase. The following sections describe several types of CVD chemical reactions.

Silane/Oxygen Thermal CVD

Silane is a gaseous compound at room temperature, which is quite stable in its pure form. However, when it is mixed with oxygen, it becomes highly volatile and will readily burn or explode with mild jarring. Great care must be taken when handling a silane-oxygen mix. In this process, silane and pure oxygen are mixed together and exposed to a substrate at a temperature of 350°C. The reaction proceeds as follows:

$$SiH_{4(g)} + 2O_{2(g)} \longrightarrow SiO_{2(s)} + 2H_2O_{(g)} \qquad (3)$$

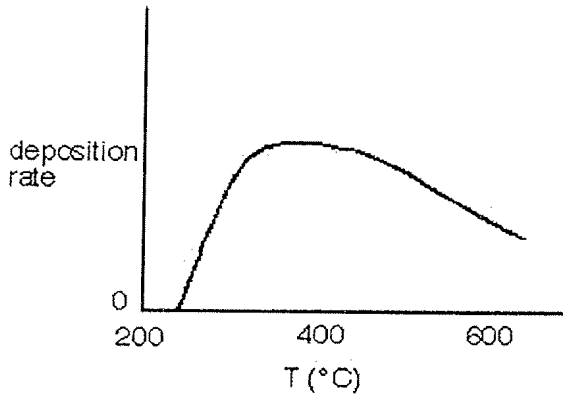

Figure 3: Silane Deposition Rate

TEOS/Oxygen Thermal CVD

The formal chemical name for TEOS is tetraethylorthosilicate. It is an organic compound that is liquid at room temperature, with flammability and toxicity properties similar to that of alcohol. In order to prepare TEOS for the chemical reaction, it must be heated and vaporized with a bubbler or liquid injection system. One of the advantages to using TEOS over silane is that with TEOS, the silicon atom is already oxidized. Therefore, the chemical conversion of TEOS to silicon dioxide is merely a rearrangement of the atoms, and no oxidation occurs. The enthalpy of the reaction is reduced. This reaction proceeds at a temperature between 650 and 850°C, and it can take place in an inert atmosphere. However, an excess of oxygen in the reactant gases increases the deposition rate.

$$Si(C_2H_5O)_{4(g)} \longrightarrow SiO_{2(s)} + 2H_2O_{(g)} + 4C_2H_{4(g)} \quad (4)$$

TEOS/Ozone Thermal CVD

Using TEOS with oxygen is a safe, reliable way to achieve silicon dioxide deposition, but the main drawback is that is requires a temperature of about 750°C to do so. One of the ways to lower the required reaction temperature is to use a more aggressive oxidant. One of the more successful compounds for this has been ozone, O_3. By adding ozone to the oxygen stream in a TEOS CVD reaction, a temperature of only 300 to 400°C is required. This temperature is much less than that required when using only pure oxygen. The reaction proceeds in a similar manner as before, but the ozone attacks the TEOS in the following manner and produces an intermediary step:

$$SiOCH_2CH_{3(g)} + O_{3(g)} \longrightarrow SiOH_{(g)} + CH_3CHO_{(g)} + O_{2(g)} \quad (5)$$

Low Pressure CVD: Tube Reactor

CVD processes are traditionally run at a low pressure in order to guarantee a steady rate of layer growth, and to ensure that the gas molecules achieve sufficient penetration into the substrate material. The reactor consists of a long horizontal tube and a piece of apparatus known as a pure

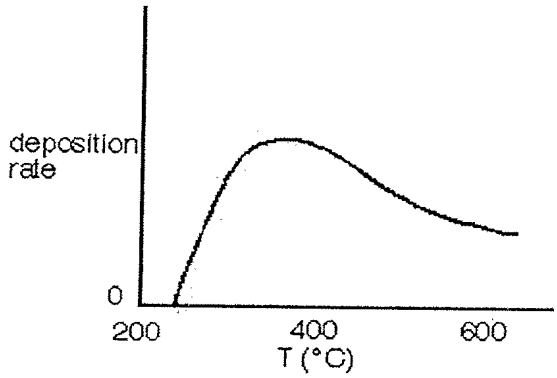

Figure 4: TEOS Deposition Rate

quartz "boat". The boat holds a batch of silicon wafers, as many as 100 to 200 may be processed at one time. It is designed to allow easy insertion of the wafers into the reactor without touching any of the sides, by suspending it on a cantilever device. The wafers are stacked on the boat just close enough to ensure that sufficient gas transport can occur on each surface. The furnace tube is surrounded by 2 or more sets of independently controlled heating coils. They facilitate the creation of a temperature gradient along the furnace, if one is needed. Also, they must be very accurate in their ability to control the temperature, to within one degree Celsius. The furnace has a gas inlet for the precursors and an outlet for the product gases that need to be expelled. Since the reaction occurs at low pressure, the openings must be sealed with polymeric o-rings and endcaps. These must be specially cooled to contend with the high process temperatures of the reaction. Also, a vacuum pump is required to create the low pressure environment. One of the problems with this type of furnace is that the oxide is deposited on everything in the reactor. Therefore, they require extensive cleaning at periodic intervals.

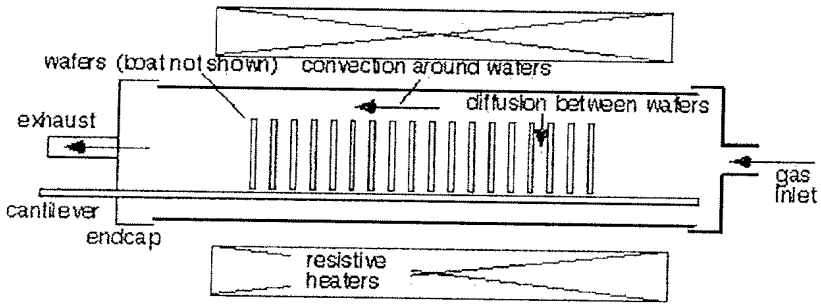

Figure 5: CVD Tube Reactor

Atmospheric Pressure CVD: Injector-based Reactor

This reactor uses a multiport gas injection system that mixes the reactant gases together at the instant they are dispensed into the deposition region. It injects the gases at a very high velocity, so that the highly reactive mixtures of reactants like silane and oxygen can be used at atmospheric pressure. This technique eliminates the burden of having a dust-tolerant vacuum pumping system to achieve a low pressure. The quality of the thin oxide produced is good, comparable to that of the LPCVD reactor. The injection gas nozzles are aimed directly at a wafer, which travels below them on a flexible metal belt. The wafers are processed in this continuous manner to ensure uniform deposition. They are unloaded at the end of the process, and the metal belt is cleaned on its return path. The reactant gases used in this process must be contained to the deposition region, so large flows of pure nitrogen gas are dispensed between chambers to expel any excess reactants. This reactor has the advantage of being a continuous process with high throughput, so there is no delays due to loading of wafer batches. However, the reactor size must be large enough to allow wafers to heat up before entering and cool down before unloading.

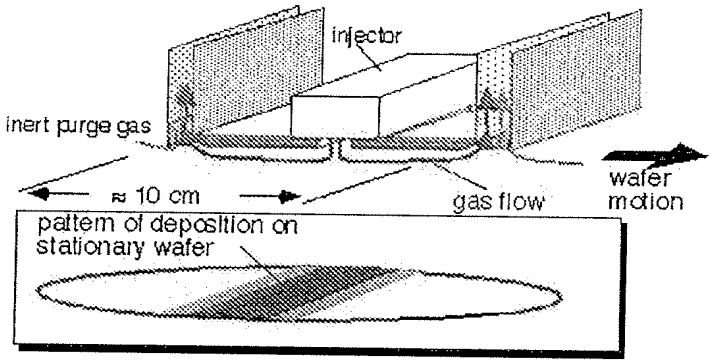

Figure 6: Injector-based Reactor

Plasma Enhanced CVD: Showerhead Reactor

A disadvantage with the previous reaction processes is that they have to be run at a high temperature, and there may be instances when a low temperature deposition process is required. One solution is to impart the reaction energy into the reactant gases, instead of heating the entire apparatus to the reaction temperature. This can be done by exposing the gas to a large electric field at a high frequency, converting the gas to plasma form. Using a high energy plasma, the reaction may proceed at a much lower temperature. The reactor vessel dispenses the reactant gases uniformly through a perforated planar surface onto a second parallel planar surface below, upon which the wafers rest. This reactor can be used for both multi-wafer batch processing and for deposition of a single wafer. The only part of the reactor that needs to be heated to the reaction temperature is the surface holding the substrate. Inside the reactor, a strong electric field causes a plasma ignition between the perforated showerhead, which also serves as an electrode, and a second electrode, namely the substrate holder. A very important design consideration in this type

of reactor is the distance between the electrodes, known as *Hc*. It influences such parameters as residence time, consumption time and radial velocities. Also, it controls the radial uniformity of the deposited film thickness. Therefore, it is important to be able to adjust the *Hc* of a reactor to change any of these variables. Another way of controlling the deposition uniformity is to change the hole configuration of the showerhead.

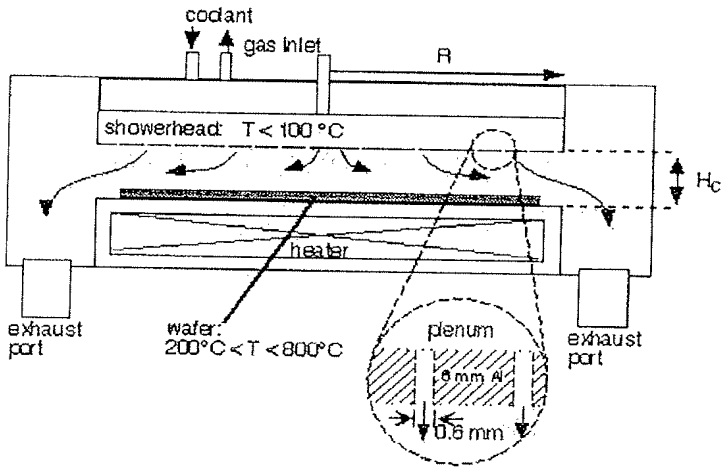

Figure 7: Showerhead Reactor

Conclusions

This paper discussed several different methodologies of producing a thin film of silicon dioxide on a substrate wafer. The two main categories covered were thermal oxidation and chemical vapor deposition. The chemistry involved with each technique was investigated, as well as the type of reactants used. The type of equipment used for each process was researched and reported. The technologies were compared to discover the advantages and disadvantages of each one.

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